Listing of Claims:

1. (Currently amended) An apparatus for dynamic power control of a processor based on a thermal condition, comprising:

a sensor to measure a thermal characteristic of a processor with a clock frequency;

a circuit, responsive to the measured thermal characteristic satisfying a pre-determined threshold, to reduce the clock frequency of the processor, the circuit including a performance demanding level input to determine ~~a level of sensitivity for~~ a rate of the frequency reduction.

2. (Original) The apparatus of claim 1, wherein the thermal characteristic includes temperature and rate of temperature change.

3. (Original) The apparatus of claim 1, wherein the circuit includes a frequency generator and a logic circuit.

4. (Original) The apparatus of claim 1, wherein the circuit reduces the clock frequency by less than fifty percent.

5. (Original) The apparatus of claim 1, wherein the circuit reduces the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency.

6. (Original) The apparatus of claim 1, wherein the sensor and circuit produce a higher operating temperature for the processor.

7. (Currently amended) A method for dynamic power control of a processor based on a thermal condition, comprising:

measuring a thermal characteristic of a processor with a clock frequency;

reducing the clock frequency in response to the measured thermal characteristic satisfying a pre-determined threshold, and ~~based on determining a level of sensitivity for~~ in accordance with a performance demanding level input value that determines a rate of frequency reduction.

8. (Original) The method of claim 7, wherein the step of measuring includes measuring temperature and rate of temperature change.

9. (Original) The method of claim 7, wherein the step of reducing includes reducing the clock frequency by less than fifty percent.

10. (Original) The method of claim 7, wherein the step of reducing includes reducing the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency.

11. (Original) The method of claim 10, wherein the step of reducing includes reducing the clock frequency in response to the measured thermal characteristic satisfying a pre-determined threshold to produce a higher operating temperature of the processor.

12. (Currently amended) A method for using control logic to provide dynamic power control of a processor based on a thermal condition, comprising:

entering a first state from a second state in response to a measured thermal characteristic of a processor with a clock frequency failing to satisfy a first pre-determined threshold where the first state outputs the clock frequency for the processor and the second state reduces the clock frequency for the processor;

remaining in the first state in response to a measured thermal

characteristic of the processor failing to satisfy the first pre-determined threshold; and

entering the second state from the first state in response to a measured thermal characteristic of the processor satisfying the first pre-determined threshold, and ~~based on determining a level of sensitivity for~~ in the second state, performing frequency reduction in accordance with a performance demanding level input value that determines a rate of frequency reduction.

13. (Original) The method of claim 12, wherein the thermal characteristic of the processor includes temperature and rate of temperature change.

14. (Original) The method of claim 12, further comprising:

entering a third state from the first state in response to a measured thermal characteristic of the processor satisfying a second pre-determined threshold where the third state waits for a measured thermal characteristic of the processor to satisfy a third pre-determined threshold to reduce the clock frequency for the processor;

remaining in the third state in response to a measured thermal characteristic of the processor failing to satisfy the third pre-determined threshold; and

entering the first state from the third state in response to a measured thermal characteristic failing to satisfy the second pre-determined threshold.

15. (Original) The method of claim 14, wherein the second pre-determined threshold is a temperature threshold, and the third pre-determined threshold is a rate of temperature change threshold.

16. (Original) The method of claim 14, further comprising:

entering the second state from the third state in response to a measured thermal characteristic of the processor satisfying the third pre-determined threshold;

remaining in the second state in response to a measured thermal characteristic of the processor satisfying the third pre-determined threshold; and

entering the third state from the second state in response to a measured thermal characteristic of the processor failing to satisfy the second pre-determined threshold.

17. (Original) The method of claim 16, wherein the second pre-determined threshold is a temperature threshold, and the third pre-determined threshold is a rate of temperature change threshold.

18. (New) A processor comprising:

thermal sensing logic to output function signals taking on values representing a function of a temperature and a rate of temperature change, and an enabling signal taking on values responsive to whether the function signals meet or do not meet predetermined temperature and rate of temperature change thresholds;

performance demanding level logic to output a signal taking on values that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second; and

frequency reduction logic coupled to the performance demanding level logic and the thermal sensing logic, to perform frequency reduction based on the values generated by the thermal sensing logic and the performance demanding level logic.

19. (New) The processor of claim 18, wherein the function signals and the enabling signal and associated logic implement a state machine to cyclically enter one of first, second and third states, the first state corresponding to a condition wherein the function signals indicate that the predetermined temperature and rate of temperature change thresholds are not met and therefore frequency reduction is not performed, the third state corresponding to a condition wherein the function signals indicate that the predetermined temperature and rate of temperature change thresholds are met and therefore frequency reduction is performed, and the second state corresponding to a condition wherein one of the predetermined temperature threshold and the predetermined rate of temperature change threshold is met but the other is not, each of the first, second and third states being enterable from the other states.

20. (New) The processor of claim 18, wherein values output by the performance demanding level logic are responsive to a processor application.